REMARKS

Claims are amended to correct drafting errors or in response to the Examiner's objections. Claims are not amended to reduce the scope of claims so as to avoid reading on any prior art cited by the Examiner. Each amended claim is intended to be broadly interpreted to cover all modes of practicing the invention employing the combination of elements as recited in the claim, including modes employing elements or steps that are functional equivalents of examples of such elements or steps described in the specification.

It is proposed that FIG. 9 be amended to correct a reference character error as indicated in the enclosed red-marked copy. A revised formal drawing including the proposed amendment to FIG. 9 is also enclosed as a replacement for the current version of the formal drawing if the Examiner finds the amendment to be acceptable.

The following numbered sections are provided in response to similarly numbered sections of the office action.

[1-4]

The applicant affirms election of claims 1-13.

[5]

Claim 8 is objected to under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a preceding claim, and claim 8 is amended in response to this objection.

[6-11]

Claims 1-5 and 9-13 are rejected under 35 USC 102(e) and 102(a)as being anticipated by US Patent 6,305,001 (GRAEF). The applicant respectfully requests the Examiner to withdraw the rejections of these claims in view of the following remarks distinguishing them over GRAEF.

The applicant's invention relates to a method for synthesizing a clock tree for an IC for delivering edges of a clock signal concurrently to each of a set of syncs (clocked devices such as registers, flip-flops and the like) to be clocked by the clock signal edges.

A clock tree synthesizer in accordance with the invention separately synthesizes and independently balances a clock tree subtree T1-T4 for each base level partition P1-P4 for delivering the clock signal from a starting point S1-S4 on the perimeter of that

base level partition to all of the syncs residing within the partition. Note that while every subtree T1-T4 is balanced in that it provides substantially the same delay from its starting point S1-S4 to the syncs within the partition, the subtrees T1-T4 need not provide the same delays. For example subtree T2 may take longer to deliver the clock signal from its starting point S2 to the syncs in partition P2 than subtree T4 requires to deliver the clock signal from its starting point S4 to the syncs in partition P4. After synthesizing and balancing the subtrees T1-T4, the synthesizer generates a top level portion of the clock tree residing within top level partition P0 for delivering the clock signal from an IC node N5 to the starting node S1-S4 on the perimeter of each partition P1-P4. The synthesizer designs the top level portion of the clock tree to compensate for differences in delays of subtrees T1-T4 so that clock signal edges arrive at all syncs within all partitions at substantially the same time.

The applicant's invention thus relates to synthesizing a clock tree for an IC that has been partitioned according to layout area with syncs being assigned to partitions in accordance with the area in which they reside. The clock tree that the applicant's invention produces delivers clock signal edges to all syncs at substantially the same time regardless of which partition each sync resides in.

GRAEF also describes a method for synthesizing a clock tree involving "partitioning" an IC design with respect to the syncs, but GRAEF partitions the IC in a different way, and for a different reason. GRAEF teaches that in some ICs not all syncs are to receive clock signal edges at the same time. As illustrate in GRAEF's FIGs. 7 and 9, GRAEF's clock tree is designed to deliver clock signal edges to various groups of syncs at different times (i.e. with different phases). Thus to synthesize a clock tree, GRAEF assigns the syncs into several "clock signal distribution groups" wherein each group corresponds to a separate clock signal phase and wherein syncs are assigned to each group according to the clock phase with which they are to be clocked. The necessary clock phase difference between the groupss is provided delay devices that are external to the groups. See for example FIG. 9 where the phase differences between groups 404, 406 and 408 is provided by buffer 412 and 414. Thus GRAEF's clock tree synthesis system organizes the syncs of an IC not according to the <u>area or partition of the layout</u> in which they reside as does the applicant's synthesis system, but in

accordance with the clock signal phase with which they are to be clocked.

Claim 1

The applicant's claim 1 preamble recites that the IC layout comprises a set of base level partitions and a top level partition with all of the partitions occupying separate areas of the IC's substrate. Claim 1 then recites that a separate subtree for each partition is separately synthesized and independently balanced. Claim 1 is distinguishable over GRAEF because GRAEF does not teach separately synthesizing and independently balancing subtrees for partitions occupying separate areas of an IC layout. GRAEF teaches generating a clock tree for an IC design wherein syncs are grouped according to clock phase.

Also GRAEF does not teach independently synthesizing and balancing subtrees serving the syncs assigned to each group. Since the subtrees supplying all of groups 404, 406 and 408 must have the same internal delay, they cannot be independently synthesized and balanced as recited in claim 1.

GRAEF's abstract mentions only partitioning an IC design specification such as a VHDL or RTL behavioral description of an IC (see col. 9, lines 1-11) and does not disclose partitioning an IC layout which is a description of where cells forming an IC are placed in a substrate, not a description of how they behave. Also the GRAEF's abstract says nothing about partitions relative to areas of a substrate; it speaks only about partitioning a design specification relative to differences timing with which clock recipients are to receive clock signal edges.

GRAEF's column 9, lines 11-32 teach partitioning a technology-independent description of an IC and does not disclose partitioning an IC layout as recited in claim 1 which is a technology-dependent description of where cells forming an IC are to be placed in a substrate, not a description of how cells behave. Also these lines of GRAEF say nothing about partitions relative to areas of a substrate. This section of GRAEF speaks about grouping clock recipients (syncs) relative to differences in timing with which they are to receive clock signal edges and does not speak about grouping them according to the areas of a substrate in which they are to reside. GRAEF's col. 10, lines 11-28 do not disclose an IC layout partitioned into separate areas. This section of GRAEF teaches creating a clock budget plan that indicates that clocked

devices assigned to different groups according to the relative times at which the clocked devices are to be clock, not according to an area of a layout in which they reside. GRAEF's column 11, lines 6-9 teach nothing about an IC layout comprising partitions occupying separate areas of the layout--they discuss how separate groups of clocked devices must be clocked at different times. GRAEF's col. 12, lines 6-56 teach nothing about an IC layout comprising partitions occupying separate areas of the layout. This section of GRAEF teaches instead that clocked devices included in a gate-level description of an IC should be assigned to timing groups in accordance with relative times at which they are to receive clock signals, not in accordance with an area of an layout in which they are to reside. GRAEF's FIG.6 does not show an IC layout partitioned according to area. It is a flow chart showing steps of an IC process including steps of generating a technology-dependent description of an IC (step 110), partitioning that description (not a layout) into separate functional modules (step 110), synthesizing a gate level description of an IC (not a layout) (step 130) and mapping the clock recipients (step 135) into separate timing groups, not into separate area partitions of a layout. (See col. 12, lines 40-56).

GRAEF's FIG. 7 does not show an IC layout partitioned according to area. FIG. 7 is a graphical representation of a timing budget showing how different groups 210, 220, 230 and 240 of clocked devices are to receive a clock signal at different times. GRAEF's FIG. 9 does not show an IC layout partitioned according to area. It is a block diagram showing how buffers 410, 412 and 414 are arranged in series to deliver clock signal edges at different times to different groups 404, 406 and 408 of clocked devices that require clock signals edges at differential times. GRAEF's FIG. 10 does not show an IC layout partition according to area; it is a functional block diagram of a general purpose computer. See column 8, lines 46-49.

Claim 1 is therefor patentable over GRAEF because GRAEF does not teach independently synthesizing and balancing subtrees for separate areas of an IC layout as recited in claim 1.

Claim 2

Claim 2 depends on claim 1 and is patentable over GRAEF for similar reasons. Claim 2 further recites that at least two of the subtrees have dissimilar average clock signal path delays and that

the top level portion of the clock tree compensates for differences in average path delays so that clock signal edges arrive at syncs within all partitions at substantially the same time.

GRAEF teaches somewhat the opposite of this. In GRAEF's clock tree the subtrees within all all groups are to have the same average internal delay while the top level portion of the clock tree to be designed to make the clock signal arrive at syncs with different groups at substantially different times.

GRAEF's FIGs. 7, col. 10 teach nothing about subtrees having dissimilar average clock signal path delays, or about providing a top level portion of the clock tree compensates for differences in average path delays so that clock signal edges arrive at syncs within all partitions at substantially the same time. FIG. 7 is a graphical representation of a timing budget showing how different groups 210, 220, 230 and 240 of clocked devices receive clock signal edges at different times. GRAEF's column 10 teaches that clocked devices are to be assigned to timing groups according to the relative times at which they are to receive clock signal and that a top level of the clock tree is to deliver clock signals to the groups at different times so that the clocked devices in different groups will be clocked at different times.

GRAEF's FIG. 9 and col. 13, line 46 through col. 14, line 37 teaches nothing about subtrees having dissimilar average clock signal path delays, or providing a top level portion of the clock tree compensates for differences in average path delays so that clock signal edges arrive at syncs within all partitions at substantially the same time. This section of GRAEF teaches that a top level of the clock tree is to deliver clock signals to the timing groups at different times so that the clocked devices in the groups will be clocked at different times.

Claim 3

Claim 3 depends on claim 1 and is patentable over GRAEF for similar reasons. Claim 3 further recites that the top level partition also includes syncs and that a subtree is also synthesized for that partition. See for example the applicant's FIG. 9 showing that a subtree T0 is synthesized for top level partition P0.

GRAEF does not disclose any "top level" partition spanning an area of a substrate containing syncs as well as top level portions of a clock tree for supplying a clock signals to other partitions. Note as in GRAEF's FIG. 9 that the syncs are assigned to clock

distribution groups and that a top level portion of the clock tree, but no syncs, reside outside these groups.

GRAEF's col. 13, line 46 through col. 15, line 40 teaches nothing about synthesizing a subtree for syncs included in a top level partition of a semiconductor substrate as recited in claim 3. GRAEF's FIG. 9 schematically shows a top level portion of a clock tree formed by buffers 410, 412 and 414 but it delivers a clock signal to clock distribution groups organized according to relative times at which clocked devices are to be clocked, not by area, and nothing in FIG. 9 suggests providing a subtree for syncs included in a top level partition of a semiconductor substrate.

Claim 4

Claim 4 depends on claim 1 and is patentable over GRAEF for similar reasons. Claim 4 further recites that signal paths delivering the clock signal from a first node within the top level partition to starting points of subtrees of first and second partitions have dissimilar path delays "to compensate for substantially differing average clock signal path delays of the subtrees of the first and second base level partitions so that a clock signal edge departing the first node will arrive at each sync with the first and second base level partitions at substantially the same time.

GRAEF teaches somewhat the opposite of this -- that path delays within the top level portion of the clock tree should be designed to make the clock signal arrive at each syncs within different timing groups at substantially different times.

GRAEF's col. 13, line 46 through col. 15, line 40 and FIG. 9 teach nothing about a top level portion of a clock tree delivering the clock signal from a first node within the top level partition to starting points of subtrees of first and second partitions have dissimilar path delays "so that a clock signal edge departing the first node will arrive at each sync with the first and second base level partitions at substantially the same time" as recited in claim 4. This section of GRAEF and FIG. 9 teach that path delays within a top level portion of a clock tree should be designed to make the clock signal arrive at syncs within different clock groups at substantially different times. GRAEF's col. 13, lines 50-54 mainly teaches that a clock distribution network is based on a clock budget plan to provide a clock signal to clock recipients in each target timing group in a manner that the clock recipients in each target

group are clocked together at the same time. However this section of GRAEF does not teach that all clock recipients are clocked at the same time. The remainder of the paragraph (col. 13, lines 55-65) clearly indicate that clocked devices in different timing groups are clocked at different times.

Claim 5

Claim 5 depends on claim 4 and is patentable over GRAEF for similar reasons.

Claim 9

Claim 9 is patentable of GRAEF for reasons similar to those discussed above in connection with claim 1.

Claim 10

Claim 10 is patentable of GRAEF for reasons similar to those discussed above in connection with claim 2.

Claim 11

Claim 11 is patentable of GRAEF for reasons similar to those discussed above in connection with claim 3.

Claim 12

Claim 12 is patentable of GRAEF for reasons similar to those discussed above in connection with claim 4.

Claim 13

Claim 13 is patentable of GRAEF for reasons similar to those discussed above in connection with claim 5.

[12-15]

Claims 6-8 and 14-15 are rejected under 35 USC 103(a) as being unpatentable over GRAEF in view of the paper "Clock Tree Synthesis Based on RC Delay Balancing," 1992 IEEE, pages. 28.3.1, page. 175-178 (MINAMI). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following remarks distinguishing these claims over the combination of GRAEF and MINAMI.

Claim 6-8 depend on claims 1 and 4 and are patentable over GRAEF alone for reasons discussed above in connection with claims 1 and 4. The Examiner cites MINAMI as disclosing only the additional

limitations recited by claim 6-8 and correctly refrains from citing MINAMI as disclosing any of the underlying limitations of parent claims 1 and 4. Claim 6-8 are therefore patentable over the combination of GRAEF and MINAMI since neither teaches the limitations of their parent claims 1 and 4.

Claims 14 and 15 depend on claims 9 and 12 and are patentable over GRAEF alone for reasons discussed above in connection with claim 9 and 12. The Examiner cites MINAMI as disclosing only the additional limitations recited by claim 6-8 and correctly refrains form citing MINAMI as disclosing any of the underlying limitations of parent claims 9 and 12. Claims 14 and 15 are therefore patentable over the combination of GRAEF and MINAMI since neither teaches the limitations of parent claims 9 and 12.

All prior art references cited by the Examiner have been reviewed and do not appear to disclose or suggest the invention as claimed.

It is believed that in view of the foregoing amendments and remarks, the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
12670 NW Barnes Road, Suite 104
Portland, Oregon 97229

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: SILI 2282 (01-051)
Postcard: 06/03-21

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Penelope Lee Stockwell